

## REMARKS

1. Claims 1-19 are pending and stand allowed in the application. The filing of this amendment has been made after the payment of the issue fee.
2. Certain errors have been discovered in Figures 1A, 4A, 4B, 8A, 8B, and 8C of the drawings. Replacement sheets correcting these Figures are included herewith along with a marked-up copy of the drawings showing the corrections made in the replacement sheets. The following discussion describes the corrections and where support for same can be found in the original drawings and the specification. No new matter is believed entered by these corrections.

In Figure 1A, line 1C-1C represents the location in FIG. 1A where the cross sectional view shown in FIG. 1C, is derived from. Line 1C-1C in FIG. 1A is incorrect because it extends across an STI region, but the cross sectional view of FIG. 1C shows the active region, without the STI region. Thus, line 1C-1C has been corrected in FIG. 1A to depict the section of FIG. 1A from which the cross sectional view shown in FIG. 1C is derived from.

Figures 4A and 4B show the flash memory cell after forming a patterned second photoresist layer 240 over a second nitride layer 239 and etching the second nitride layer 239 using the patterned second photoresist layer 240 as a mask. Figures 5A and 5B show the memory cell in a subsequent stage of fabrication after the etched second nitride layer 239 has been used as a mask to form the poly-oxide layer 241 on exposed portions of the floating gate polysilicon layer 238. Figures 5A and 5B reveal that the patterned second photoresist layer 240 and the etched second nitride layer 239 shown in Figures 4A and

4B are the reverse of what they should be. Thus, Figures 4A and 4B have been amended to show the patterned second photoresist layer 240 and the etched second nitride layer 239 in the correct pattern, consistent with the subject matter shown in FIGS. 5A and 5B.

In Figure 8A, line 8C-8C represents the location in FIG. 8A where the cross sectional view shown in FIG. 8C is derived from. Line 8C-8C in FIG. 8A is incorrect because it does not extend far enough to depict the plurality of electrically conductive vias shown in Figure 8C and described in the specification in paragraph [0024]. Thus, line 8C-8C has been corrected in FIG. 8A to depict the section of FIG. 8A from which the cross sectional view shown in FIG. 8C is derived from.


In Figure 8B, the reference numeral 310 identifying the rectangular structures has been amended to "320" to be consistent with the detailed description in paragraph [0024] which describes "a dielectric layer 310 including a plurality of bit lines 320...formed over memory cells 300."

In Figure 8C, the reference numeral 320 identifying the electrically conductive via, i.e., the vertical column structure on the left in the figure which contacts the left side drain 280, has been amended to "330" to be consistent with the numbering in the specification. Also, this column structure has been completed where it meets the drain. Further, the metal bit line, i.e., the horizontal member connecting the two vias and identified by the other reference numeral 320 has been corrected to eliminate the notch, which is not a feature of the metal bit line.

3. Consideration of this amendment and entry of same is respectfully requested, as the amendments are needed for proper protection of the invention and do not require a substantial amount of additional work on the part of the Office.

4. No fees are due with this communication. The Commissioner is hereby authorized to charge payment of any additional filing fees required under 37 CFR 1.16 and any patent application processing fees under 37 CFR 1.17, which are associated with this communication, or credit any overpayment to Deposit Account No. 50-2061.

Respectfully submitted,



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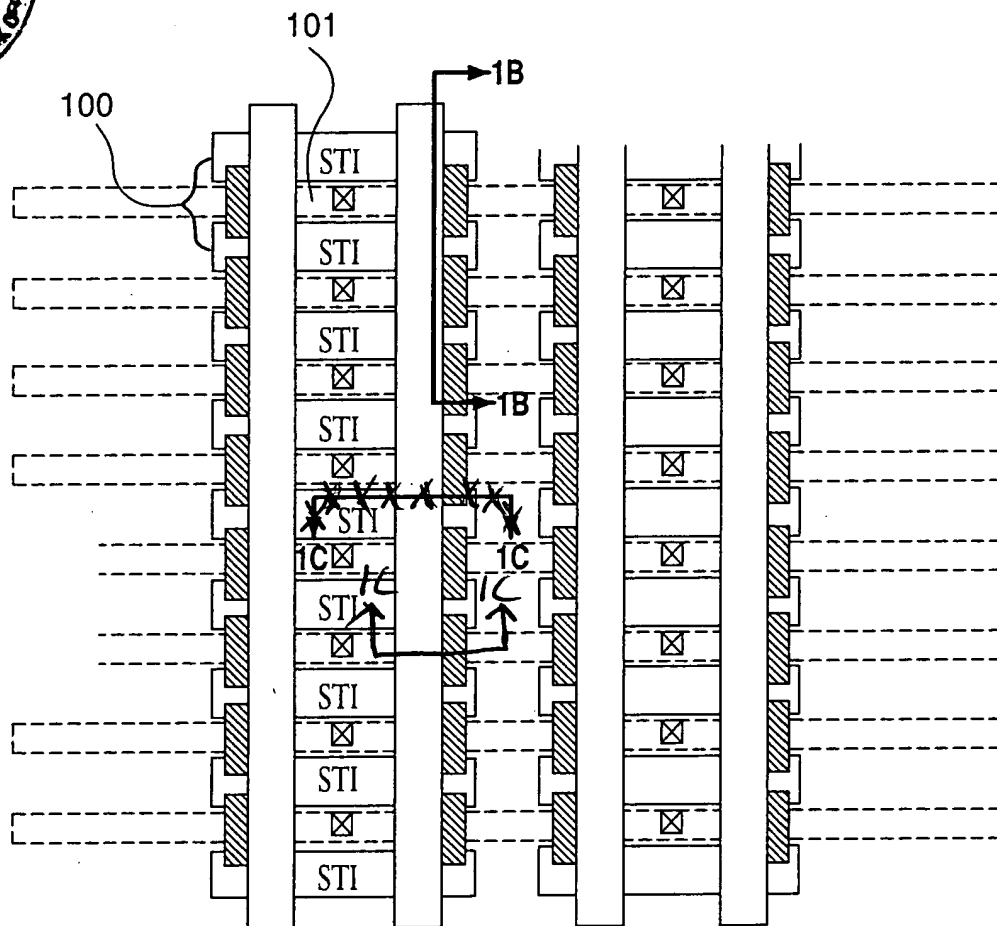


FIG. 1A

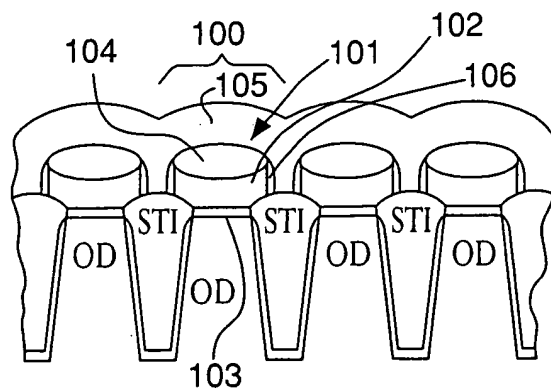


FIG. 1B

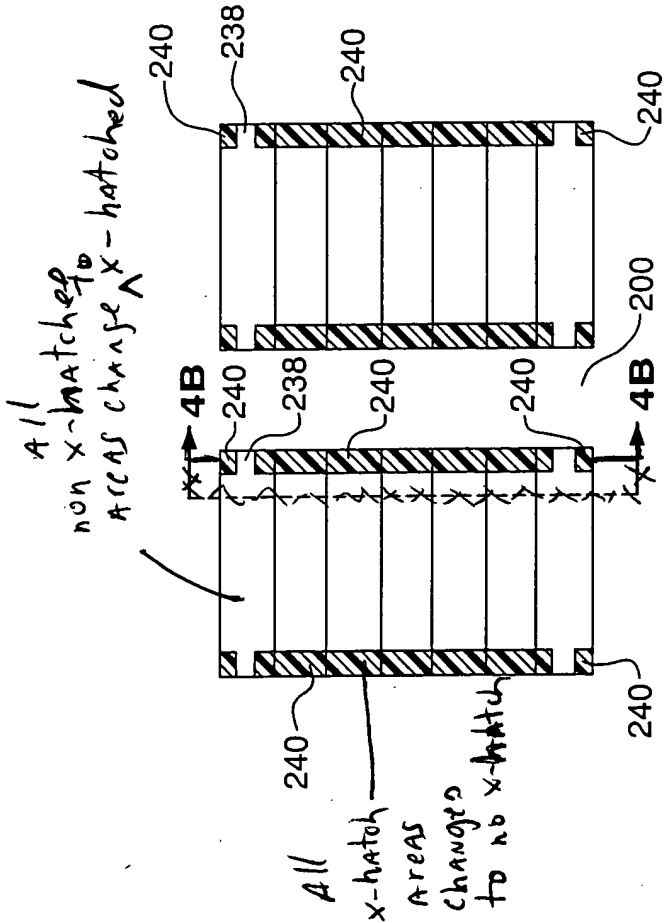


FIG. 4A

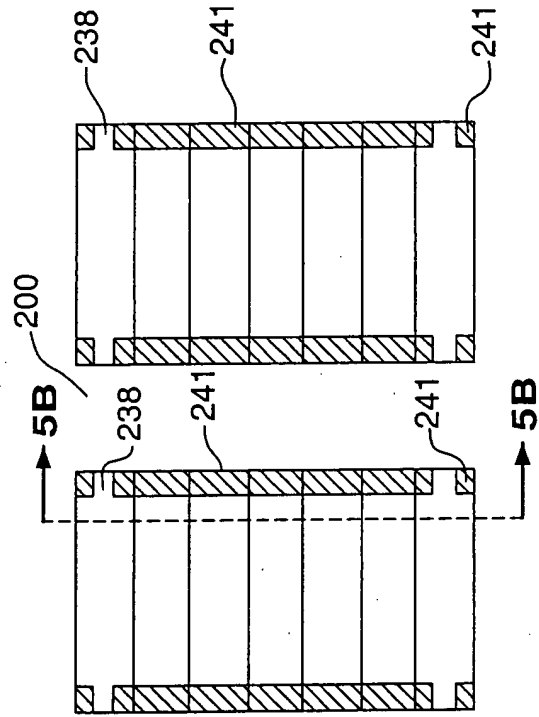


FIG. 5A

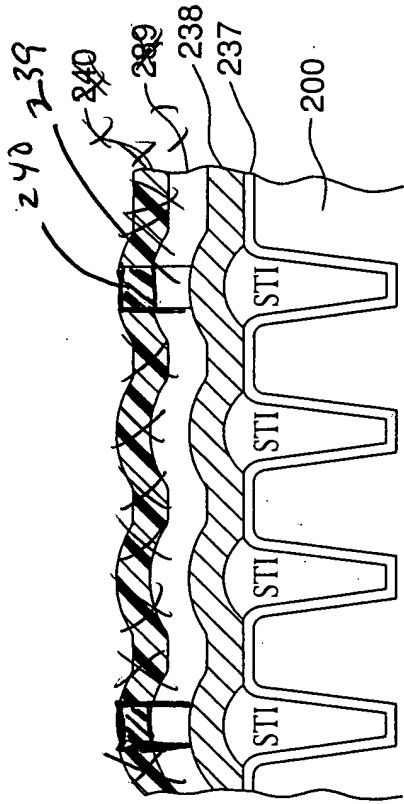


FIG. 4B

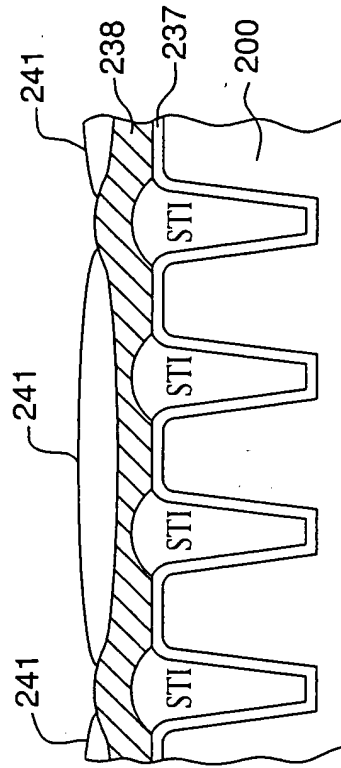


FIG. 5B

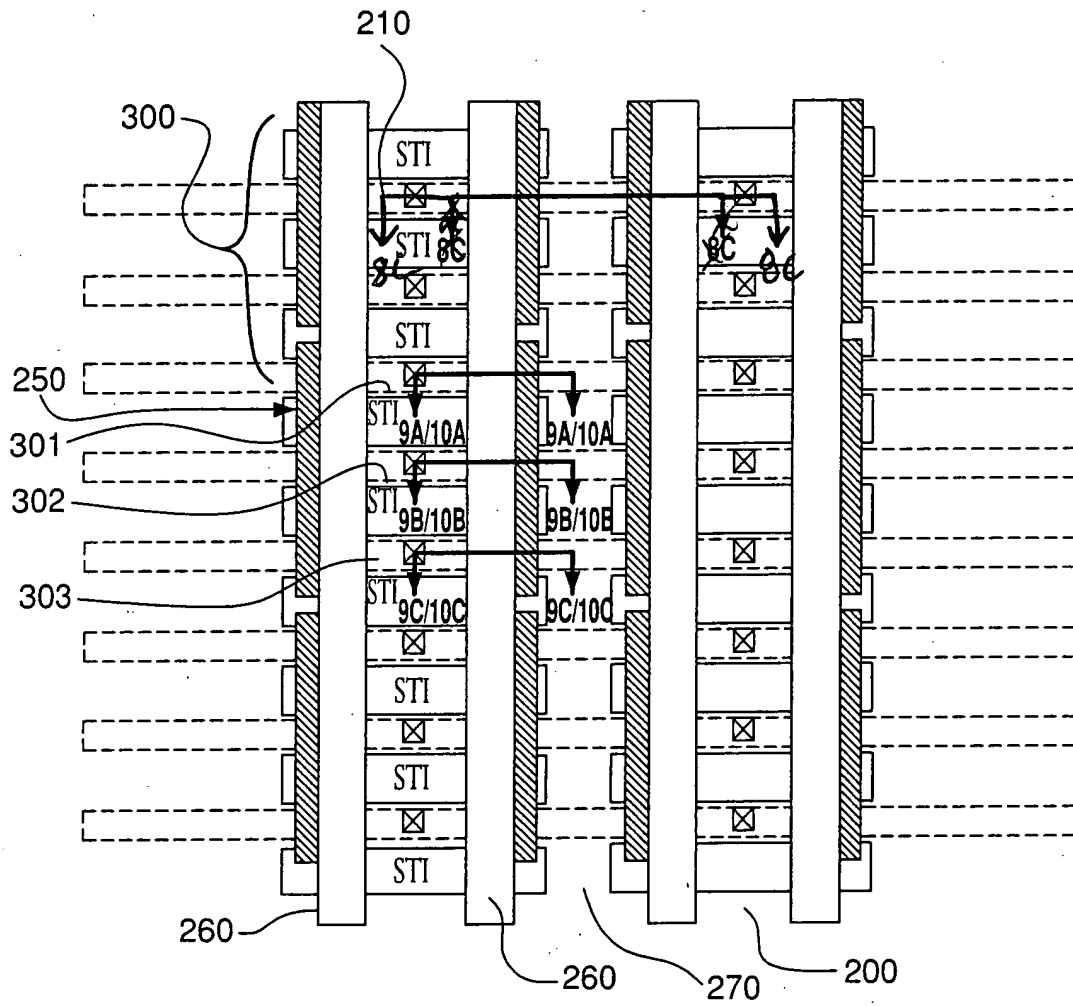


FIG. 8A

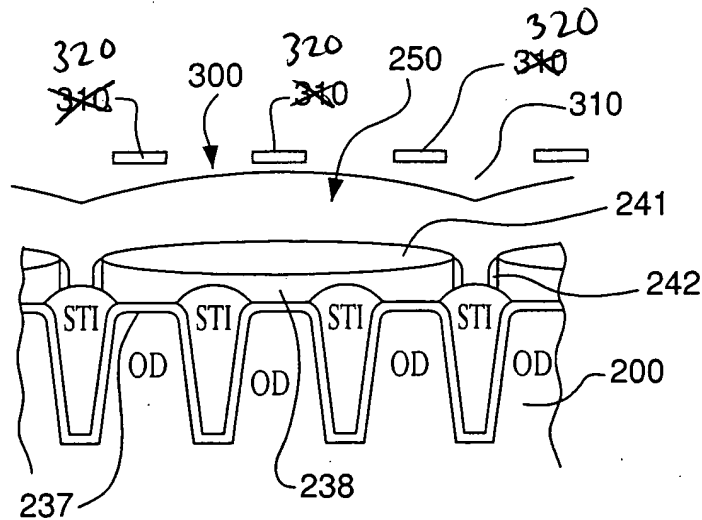


FIG. 8B

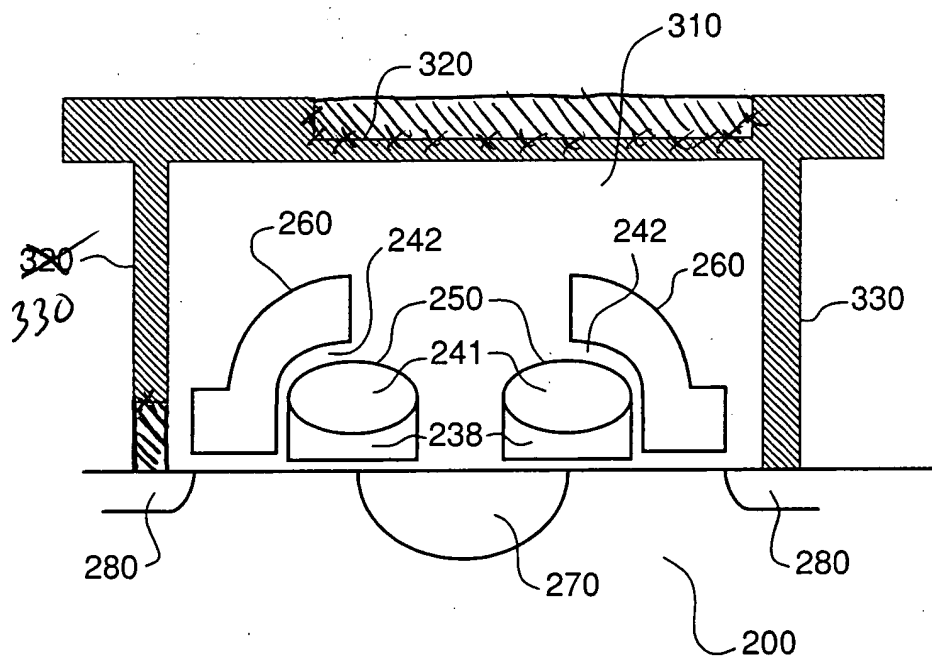


FIG. 8C